ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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Title of Invention	METHOD AND STRUCTURE FOR IMPROVING CMOS DEVICE RELIABILITY USING COMBINATIONS OF INSULATING MATERIALS

Application Number :

Confirmation Number:

First Named Applicant: Haining Yang

Attorney Docket Number: FIS920040194US1

Art Unit:

Examiner:

Search string: (5851893 or 6724053).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5851893	1998-12-22	Gardner et al.			
	2	6724053	2004-04-20	Divakaruni et al			

Signature

Examiner Name	Date